

BLF2425M6L180P; BLF2425M6LS180P

Power LDMOS transistor

Rev. 1 — 7 February 2012

Objective data sheet

1. Product profile

1.1 General description

180 W LDMOS power transistor for various applications such as ISM and industrial heating at frequencies from 2400 MHz to 2500 MHz.

Table 1. Typical performance

RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)
CW	2450	28	180	12	55

1.2 Features and benefits

- Typical CW performance at a frequency of 2450 MHz, a supply voltage of 28 V and an I_{DQ} of 10 mA:
 - ◆ Average output power = 180 W
 - ◆ Power gain = 12 dB (typ)
 - ◆ Efficiency = 55 % (typ)
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched for ease of use
- Qualified up to a supply voltage of 28 V
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

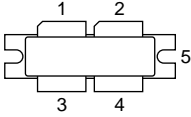
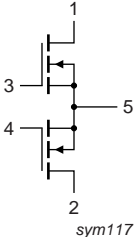
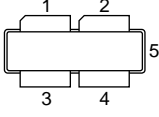
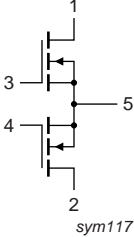
1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM and industrial heating.



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF2425M6L180P (SOT539A)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF2425M6LS180P (SOT539B)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M6L180P	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF2425M6LS180P	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_{case}	case temperature		-	150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 180\text{ W}$	0.38	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$				
		$V_{DS} = 28\text{ V}$	-	-	3	μA
		$V_{DS} = 65\text{ V}$	-	-	5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	25	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.2\text{ A}$	-	<tbd>	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5\text{ A}$	-	0.1	-	Ω

Table 7. RF characteristics

Test signal: CW; $f = 2450\text{ MHz}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 10\text{ mA}$; $T_{case} = 25\text{ °C}$ unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 180\text{ W}$	10	12	-	dB
RL_{in}	input return loss	$P_L = 180\text{ W}$	-	-10	-8	dB
η_D	drain efficiency	$P_L = 180\text{ W}$	50	55	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF2425M6L180P and BLF2425M6LS180P are capable of withstanding a load mismatch corresponding to $VSWR = <tbd>$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 10\text{ mA}$; $P_L = 180\text{ W}$ (CW); $f = 2450\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values per section.
 Z_S and Z_L defined in [Figure 1](#).

f (MHz)	Z_S (Ω)	Z_L (Ω)
2400	5.9 – j8.0	2.8 – j3.1
2450	8.4 – j7.6	2.5 – j3.1
2500	10.6 – j5.8	2.3 – j3.0

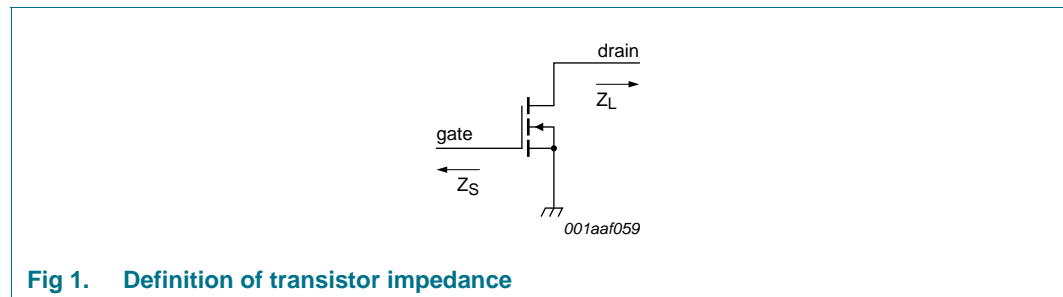


Fig 1. Definition of transistor impedance

7.3 Test circuit

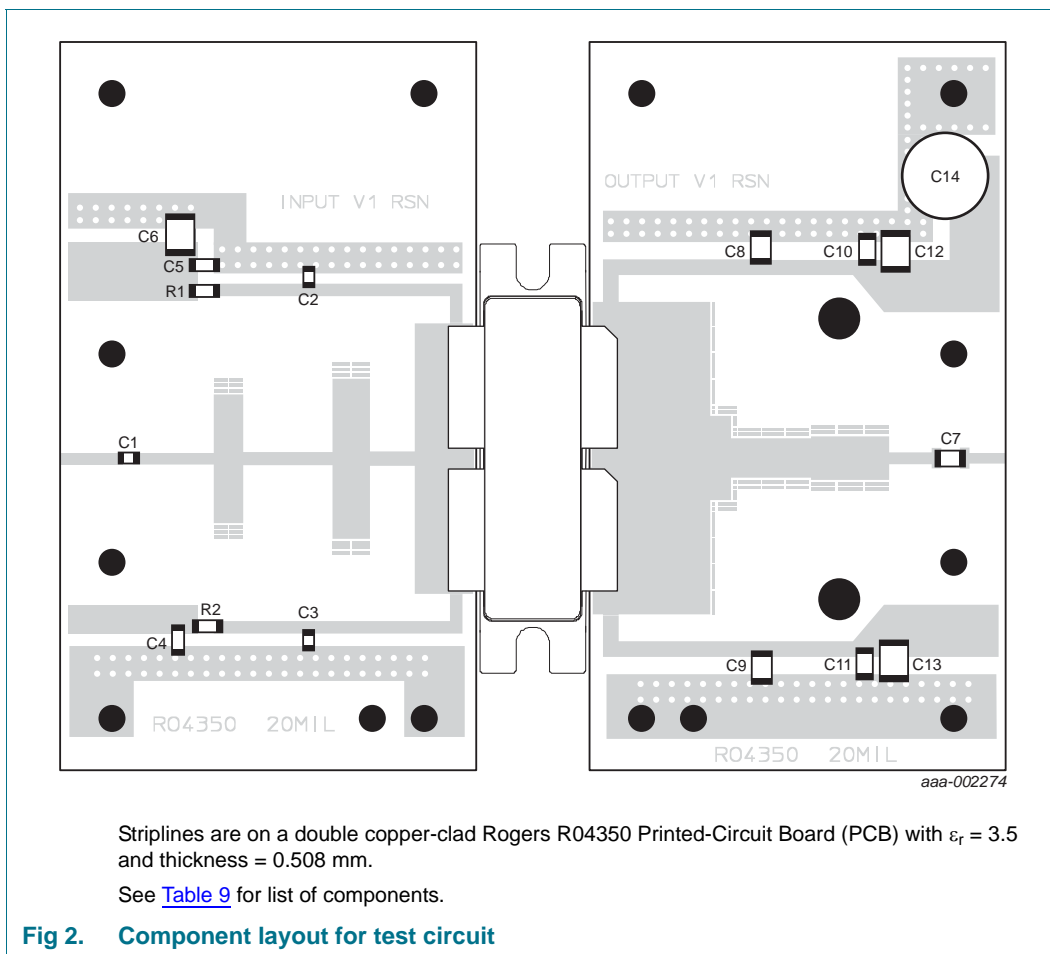


Table 9. List of components

For test circuit, see [Figure 2](#).

Component	Description	Value	Remarks
C1, C2, C3	multilayer ceramic chip capacitor	15 pF	[1]
C4, C5, C10, C11	multilayer ceramic chip capacitor	220 nF; SMD 1206	
C6, C12, C13	multilayer ceramic chip capacitor	4.7 μ F	
C7	multilayer ceramic chip capacitor	39 pF	[2]
C8, C9	multilayer ceramic chip capacitor	6.8 pF	[3]
C14	electrolytic capacitor	220 μ F, 63 V	
R1, R2	chip resistor	6.2 Ω ; SMD 1206	

[1] American technical ceramics type 100A or capacitor of same quality.

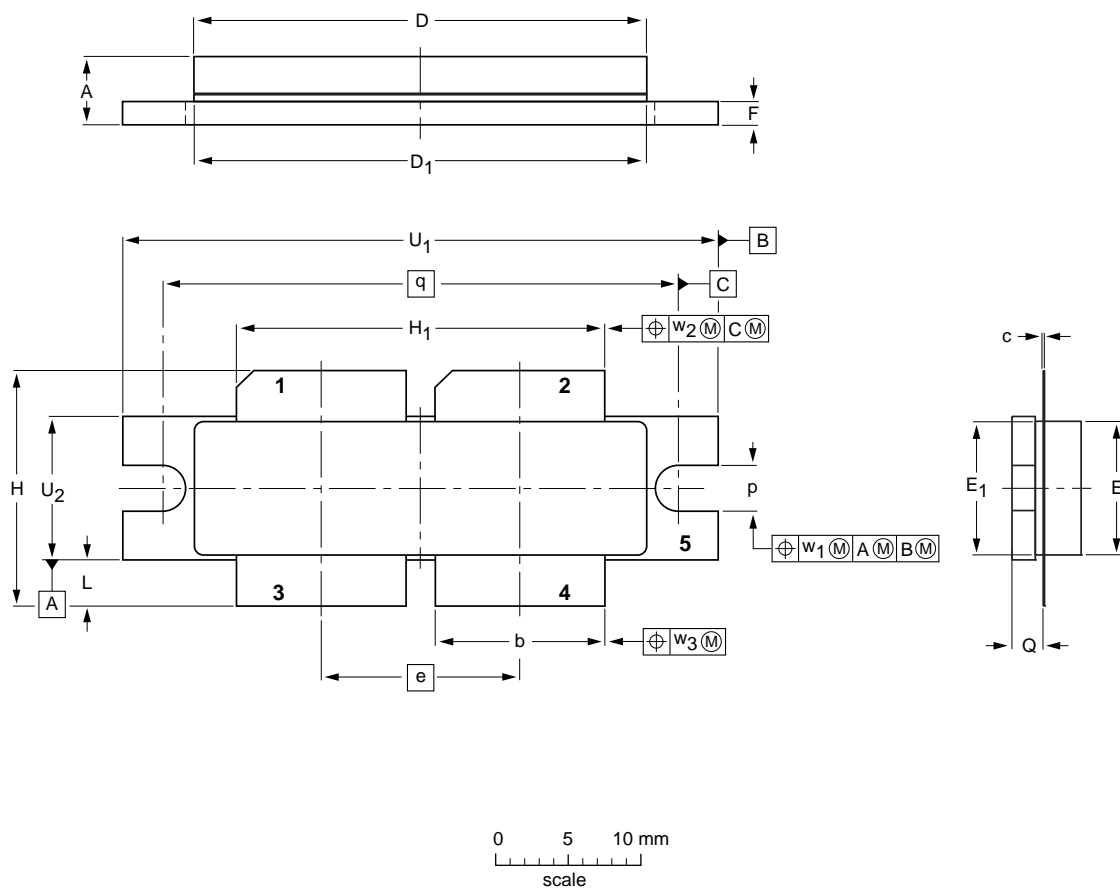
[2] American technical ceramics type 800B or capacitor of same quality.

[3] American technical ceramics type 100B or capacitor of same quality.

8. Package outline

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads

SOT539A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						00-03-03 10-02-02

Fig 3. Package outline SOT539A

Earless flanged balanced LDMOST ceramic package; 4 leads

SOT539B

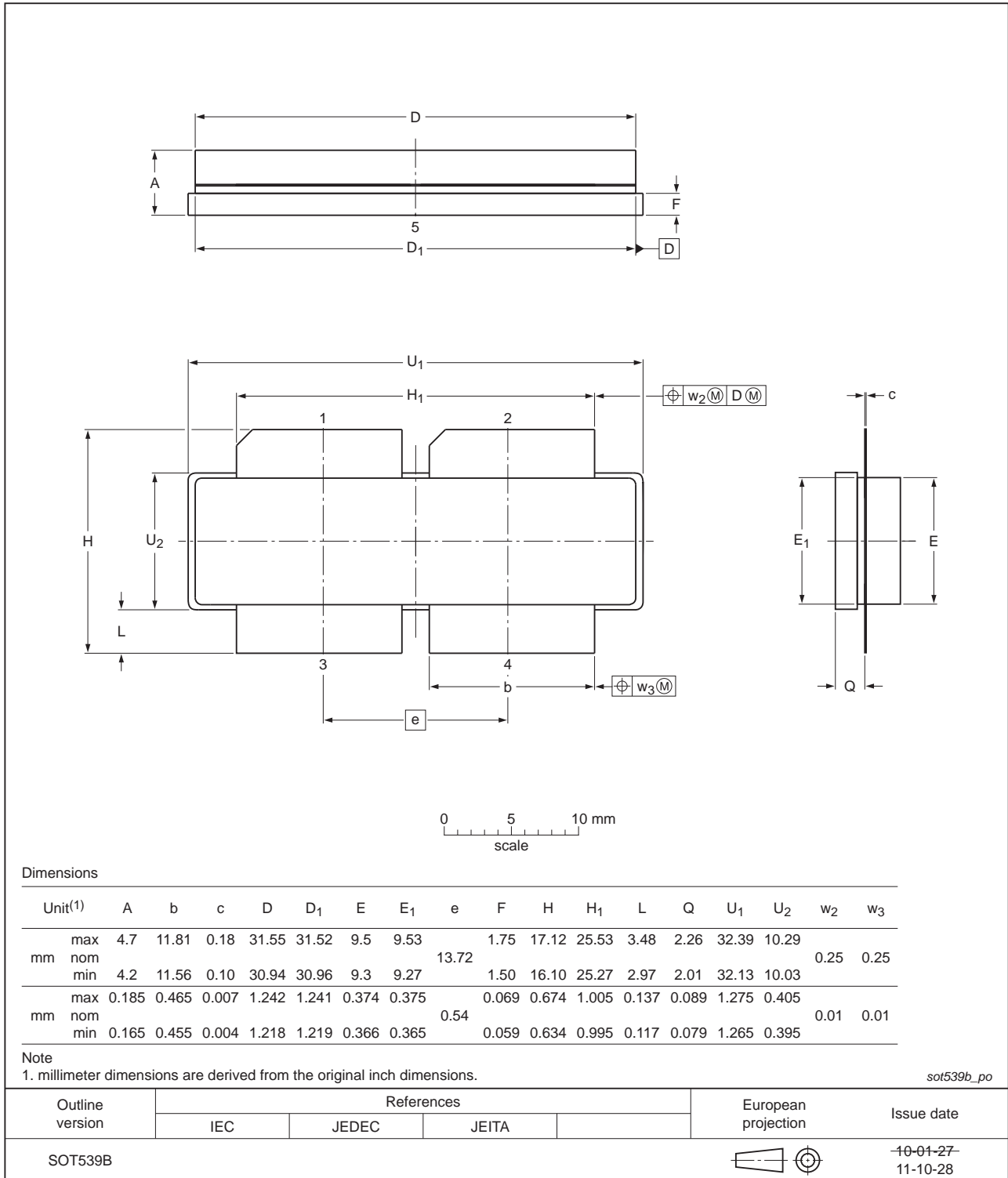


Fig 4. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
DC	Direct Current
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M6L180P_25M6LS180P v.1	20120207	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 7 February 2012

Document identifier: BLF2425M6L180P_25M6LS180P